

HIGH DEFINITION AUDIO (HDA) CODEC LAYOUT GUIDE***Introduction***

To ensure maximum performance from the High Definition Audio (HDA) codec, proper component placement and routing are very important. This document includes properly isolating the digital circuitry and analog circuitry,

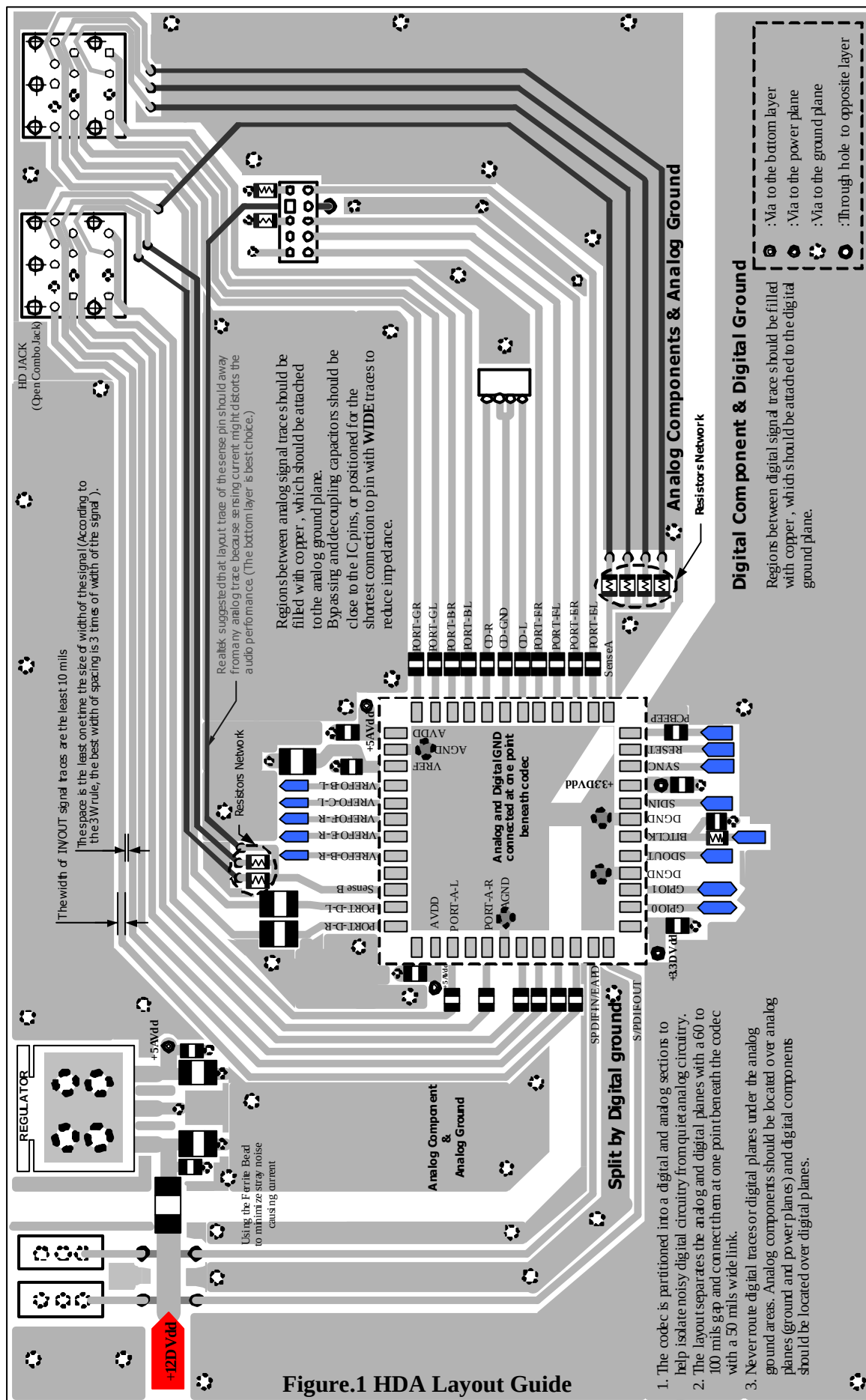
The effects of ground and supply plane geometry, decoupling/bypassing/filtering capacitors placement priorities, LINK signals, analog power supplies, and analog ground planes.

The layout design of Ground and Supply plane Geometry

Figure.1 shows a top view layout for onboard HDA codec. The layout separates the analog and digital ground planes with a 60 to 100 mils gap. The moat helps to isolate noisy digital circuitry from quiet analog audio circuitry. *The digital and analog ground planes are tied together by a wide link, about 50mils, at one point and only one point beneath the codec.* This will be the "drawbridge" that goes across the moat. Do not allow any digital or analog signal traces pass through the drawbridge, otherwise, the digital noise may be induced into the analog signals, makes audio performance worse. Similarly, NO SIGNALS WHATEVER are permitted to cross the moat (to do so creates a "slot antenna" radiator which will hammer your PCB layout with crosstalk, and create huge amounts of EMI, totally defeating your purpose).

In HDA codec layout, the major difference is the JACK DETECTION. Because of during sensing procedure, each sense pin will sense the corresponding resistors network that may interfere the performance of analog signal. In order to avoid such a situation, layout must pay attention at two points: one is the resistors network should be placed as close as possible to the sense pin. Another is the layout traces between the resistors network and HDA jack should away from any analog trace because sensing current might distorts the audio performance. The bottom layer is best choice.

In additional, in order to present the best audio performance and prevent cross-talk issue from having no enough space between left and right channels. Realtek recommended to layout the width of each IN/OUT signal traces at least 10 mils and the space is the least one time the size of width of signal trace.



For a layout that helps to reduce noise, separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. In addition to ground planes scheme, digital and analog power supply planes should be partitioned directly over their respective ground planes. Placing analog power coincident with analog ground, and digital power coincident with digital ground (as Figure.2 – Recommended separation). If any portions of analog and digital plane overlap, the distributed capacitance (result from power plane reference to ground plane or signal plane reference to ground plane) between the overlapping portions will couple digital noise into the analog circuitry. This defeats the purpose of isolated plane (as Figure.2 – wrong separation). The power and ground planes should be separated by approximately 40mils for the four layer PCB design. Using power and ground planes forming a natural, high capacitive, bypass capacitor to reduce overall PCB noise.

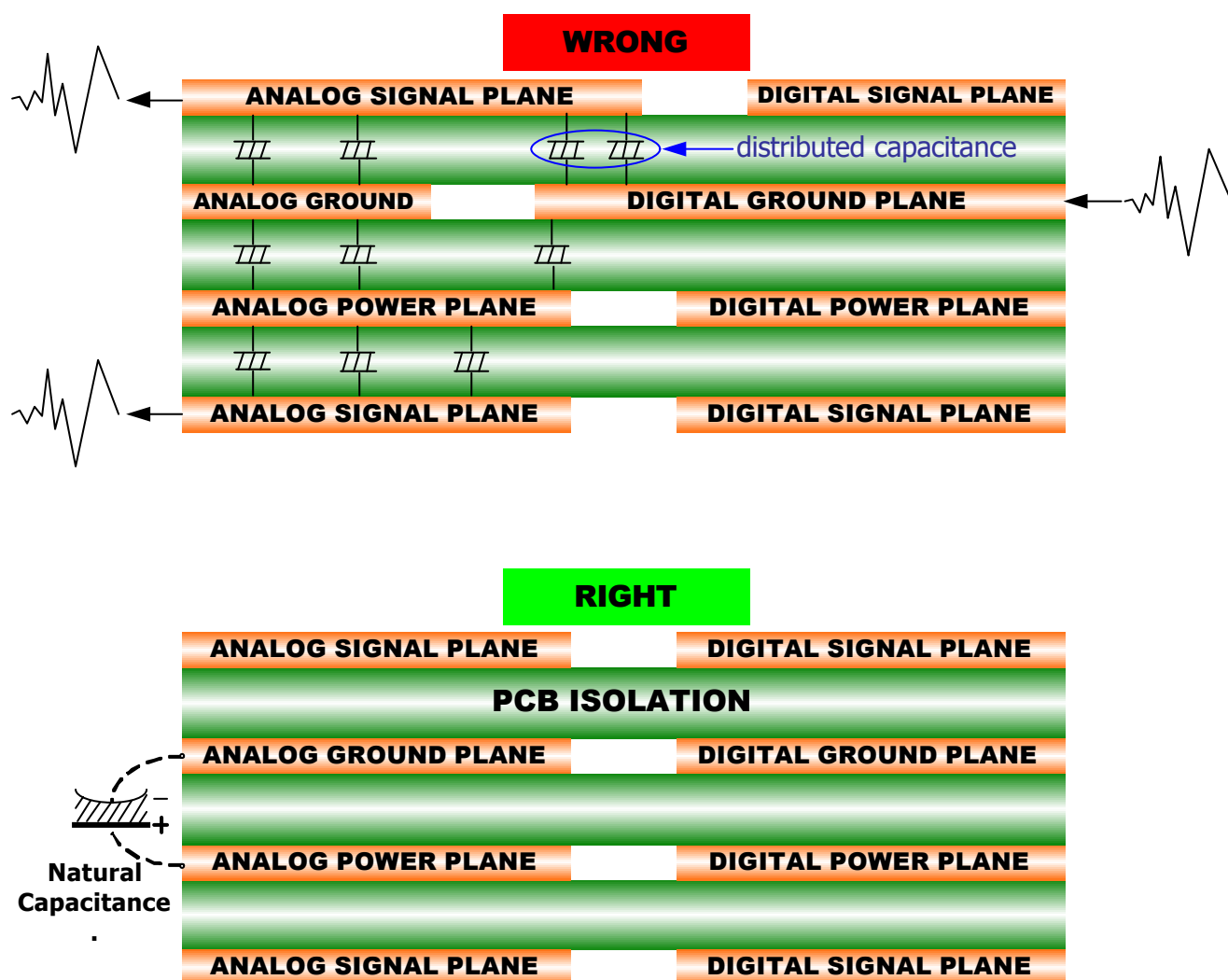


Figure.2 Cross section of PCB, the recommended separation for analog and digital plane.

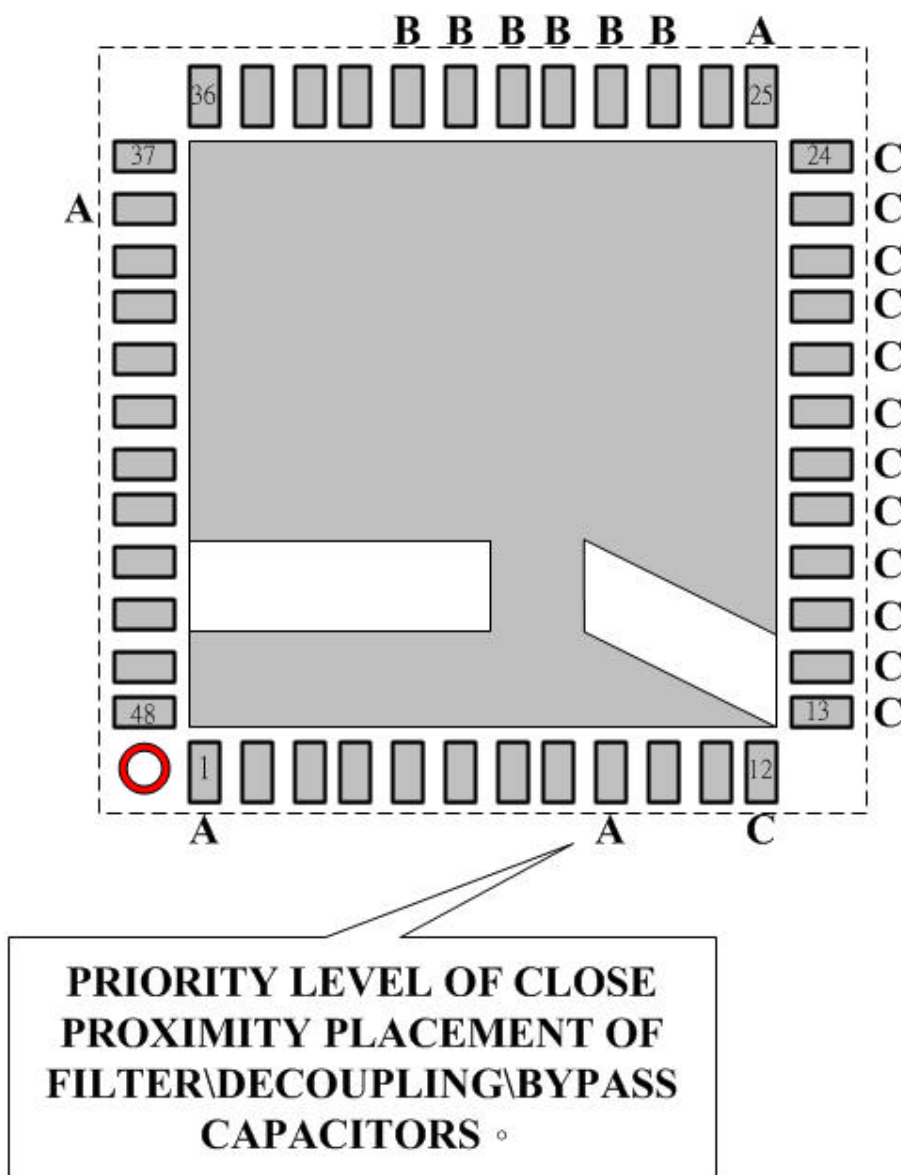


Figure.3 Recommended capacitor placement

Decoupling and bypassing capacitors

Bypass capacitors on the PCB are used to short digital noise into ground. Commonly, codec may generate noise when its internal digital circuitry is operating. The current changes arise in the power and ground pins for the related section of the codec. The goal is to force AC currents to flow in the shortest possible loop from the supply pin through the bypass cap and back into the codec through the nearby ground pin. A bypassing circuit is supposed to be a low lead inductance between the codec and the bypass capacitors when in the operating frequency of the codec. The longer the trace – the greater the inductance. To avoid long-trace inductance effects, use the shortest possible traces for bypass capacitors, with wide traces to reduce impedance. For best performance, use supply bypass leads of less than one-half inch.

In Figure 3, Pins with a first – “A” priority components placed around the codec are the bypass caps, which are located as close as possible to the supply pins. The capacitors must have low inductance and low equivalent series resistance (ESR). Tantalum 10 μ F surface mount devices are good if they are used in conjunction with 0.1 μ F ceramics. The filter capacitors with “B” priority, the reference filter to stabilize the reference voltage for internal Ops and reference output filters should be placed close to codec. A good reference voltage is relative to good analog performance. These decoupling capacitors (“C” priority) should be close to the codec pins (pin-12 to pin-24), or positioned for the shortest connections to pins, with wide traces to reduce impedance. The Table I also point out the distribution of codec capacitor locations and placement priorities.

Table I. Capacitor placement priorities

Signal Description	Package Pins	Priority of Close Proximity to Codec Pin Placement of Filter and Decoupling Capacitors
Digital Supply Voltage , +5DVdd	1,9	A
Analog Supply Voltage, +5AVdd	25,38	A
Voltage Reference Filter(V_{REF})	27	B
Voltage Reference out (V_{REF_OUT})	28,29,30,31,32	B
Analog Signal Inputs(Decouple)	12 ~ 24	C

The LINK Trace

The LINK signals operated at 24MHz bit block rate, it is sensitive to trace length. A long trace causes a slow rising time makes operation is unstable or failed. Figure.4 describes topology configuration that has been simulated on a four layers microstrip desktop platform by INTEL. It is expected that system level simulations will be done using actual trace and board model.

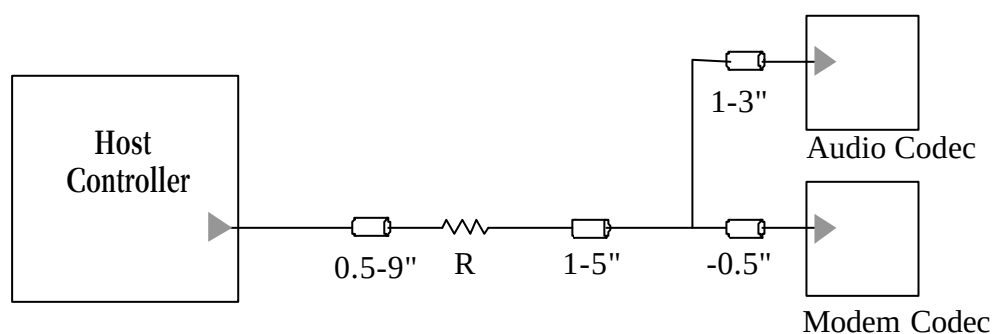


Figure 4. Recommended link trace

The Anti-Glitch Capacitors

In practical situation, it is possible that there are glitches induced on LINK signals. Glitch on RESET- generated by chipset makes a misunderstanding to reset codec in run time. Glitch on SYNC makes codec loss synchronization with chipset, analog output will be corrupted. BCLK generated by controller sometimes has ring-back or overshoot phenomenon due to impedance mismatch at receive terminal, it may cause unstable LINK operation. Figure 6 suggests system designer reserve some anti-glitch capacitors at LINK bus, Ce10 and Ce11 used to anti-glitch on SYNC and RESET-. The ring-back resistor Re6 and Ce6 are used to suppress overshoot and control slew rate on BCLK.

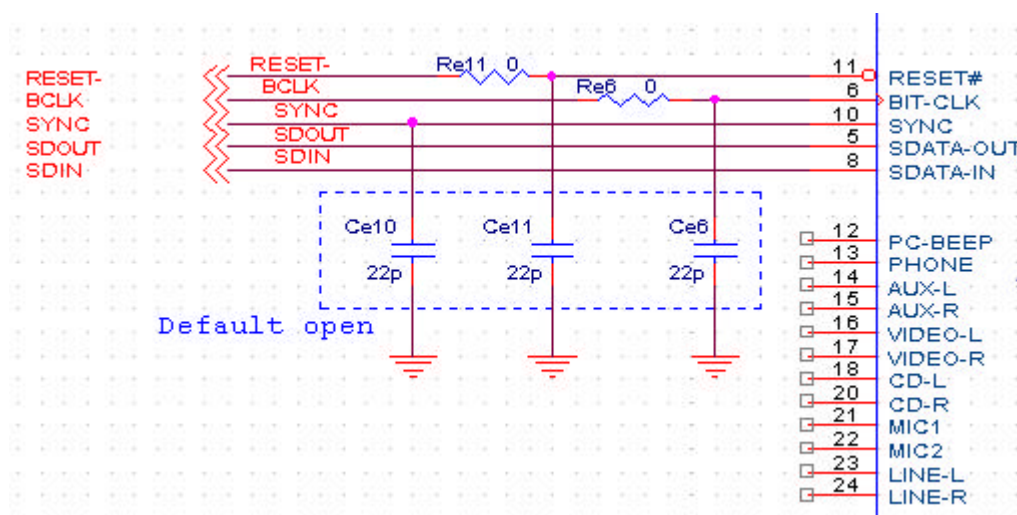


Figure 5. Reserved anti-glitch capacitors on LINK bus